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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,003	07/15/2003	Toshinori Goto	OKI 278 C1	6045

23995 7590 07/25/2005

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,003	GOTO, TOSHINORI	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/939,801.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

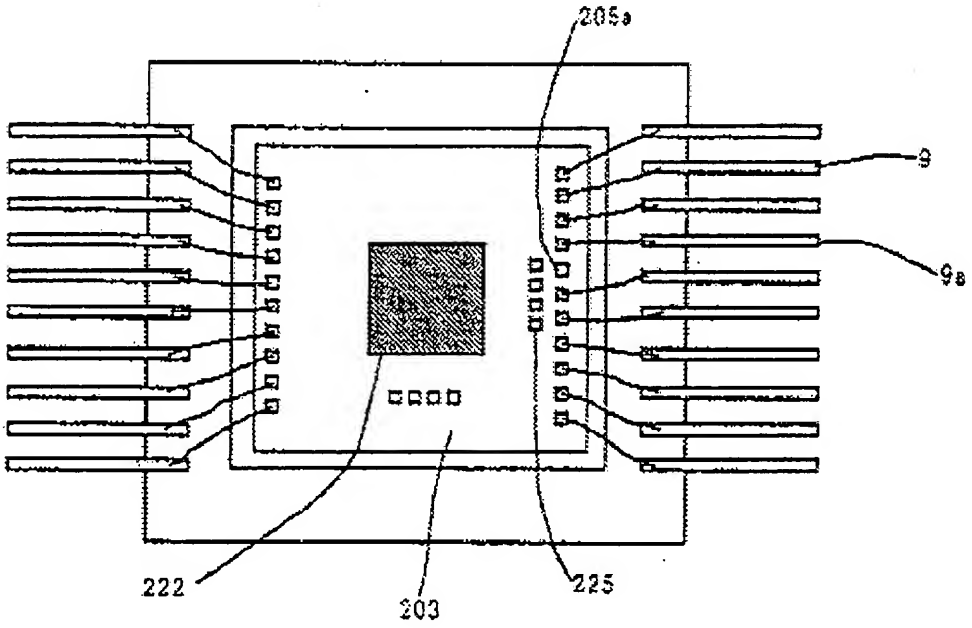
DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed May 11, 2005 have been fully considered but they are not persuasive.

2. Applicant contends that Ohie, U.S. Patent 6,580,164 B1 herein known as Ohie fails to teach or suggest that the area 103a over which the semiconductor chip is mounted (see FIG. 3), is one which is free of formation of elements which generate heat during operation as required by claim 18.

3. In response to Applicant's contention that Ohie fails to teach or suggest an area which is free of formation of elements which generate heat during operation, please note that electrical conductors near active devices in the silicon die generate more heat than the silicon areas which do not have elements, and therefore Applicant's argument is moot. Please also see FIG. 6.



4. Applicant contends that Ohie fails to disclose that the mask ROM 203 is formed specifically in an area over which the second LSI chip will be mounted as claim 19 requires.

5. In response to Applicant's contention that Ohie fails to form specifically in an area over which the second LSI chip will be mounted please see FIG. 6 above and please note that Mask ROM 222 is position over the center area of the first semiconductor chip 203 and therefore Applicant's argument is moot.

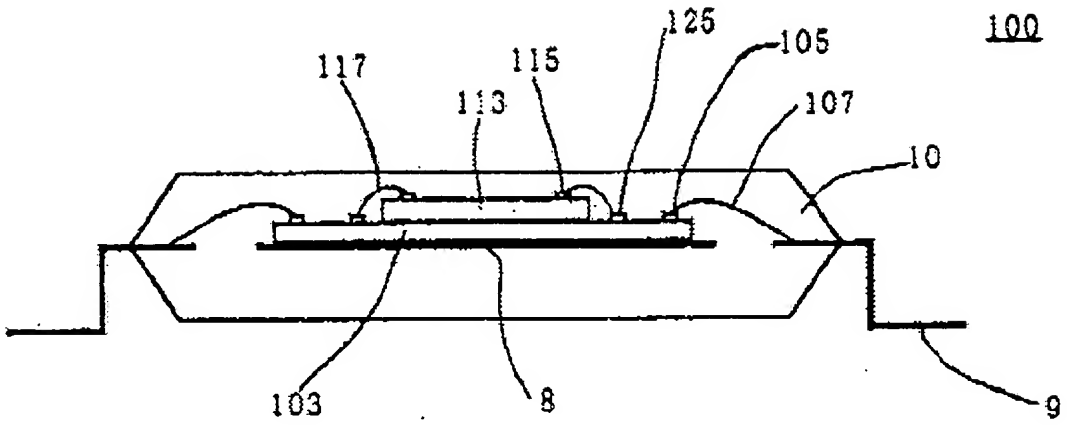
Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (f) he did not himself invent the subject matter sought to be patented.

7. Claims 18-20 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohie, U.S. Patent 6,580,164 B1.

8. Ohie discloses a semiconductor process as claimed. Please see **FIGS. 1-9**, where Ohie teaches the claimed limitations.

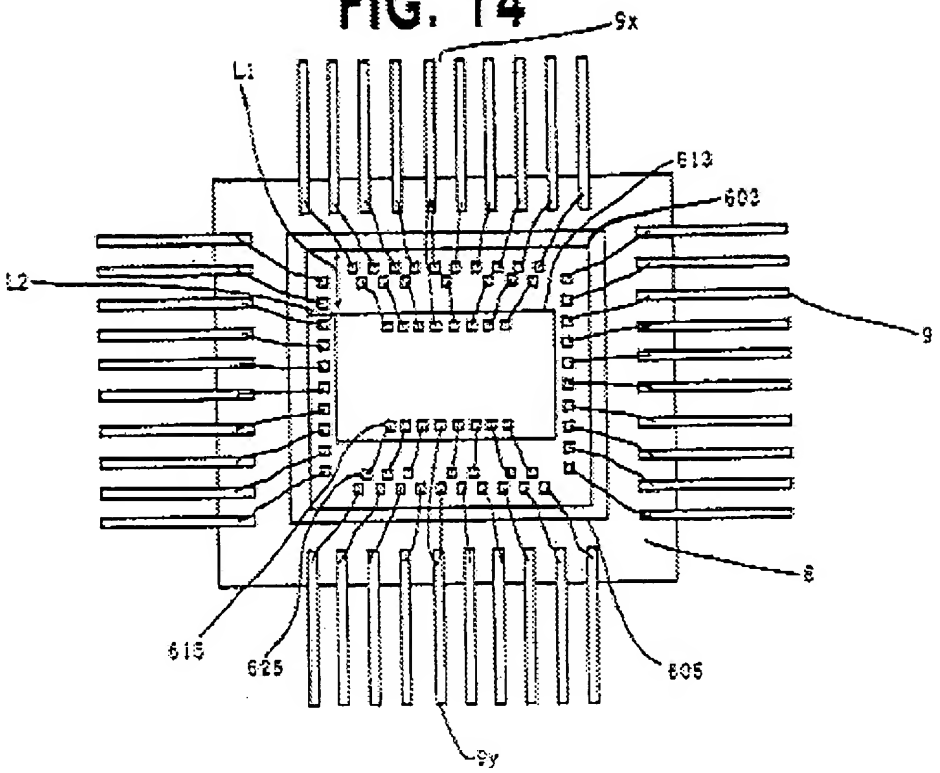


9. Pertaining to claim 18, Ohie teaches a method of manufacturing a semiconductor device having stacked semiconductor chips, comprising:

preparing a first semiconductor chip and a second semiconductor chip, the first semiconductor chip **103** having a first area which is larger than the area of the second semiconductor chip and is free of the formation of elements which generate heat when in operation, and a second area which surrounds the first area; and

mounting the second semiconductor chip on the first semiconductor chip so as to arrange the second semiconductor chip **113** to cover an area wholly within the first area of the first semiconductor chip.

FIG. 14



10. Pertaining to claim 19, Ohie teaches the method according to claim 18, wherein a microcontroller used as a mask ROM **203** is formed on the first area of said first semiconductor chip, and said second semiconductor chip serves a function of a flash memory **213**.

11. Pertaining to claim 20, Ohie teaches the method according to claim 18, wherein the first area is an approximately central area of the first semiconductor chip.

12. Pertaining to claim 22, Ohie teaches the method of claim 18, wherein the first semiconductor chip **103** has at least one first electrode **105** formed on the periphery of the first area, at least one second electrode **125** formed on the periphery of the second area, and a plurality of leads **107** disposed around said first semiconductor chip;

the second semiconductor chip **113** has at least one third electrode **115** formed thereon; and the method further comprises:

connecting the first electrode of said first semiconductor chip and the third electrode of said second semiconductor chip with at least one first metal wire; and

connecting said second electrode of said first semiconductor chip and said leads with at least one second metal wire.

13. Pertaining to claim 23, Ohie teaches the method according to claim 22, wherein said third electrode of said second semiconductor chip is electrically connected to said second electrode of said first semiconductor chip through a transistor formed within the second area of said first semiconductor chip.

14. Pertaining to claim 24, Ohie teaches the method according to claim 18, further comprising:

sealing said first and second semiconductor chips, said first and second metal wires and some of said leads with an encapsulating resin.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8100.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823